This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original): A semiconductor element comprising:

a substrate;

a first DMOS element formed on a first portion of the substrate, wherein the DMOS element includes a gate electrode having slanted side walls; and

a first MOS element formed on a second portion of the substrate that is separate from the first portion.

Claim 2 (Original): The semiconductor element of claim 1, wherein the slanted side walls of the gate electrode of the first DMOS element and side walls of a gate electrode of the first MOS element have different profiles.

Claim 3 (Original): The semiconductor element of claim 1, wherein the first DMOS element includes:

a well of a first conductive type formed on the substrate;

a body region of a second conductive type formed in the well;

a source region of the first conductive type formed in the body region;

a drain region of the first conductive type formed in the well and spaced from the source region; and

a gate insulating layer formed between the well and the gate electrode.

Claim 4 (Currently Amended): The semiconductor element of claim 3, wherein a portion of one of the slanted side walls overlaps a part of the source region ~~overlaps a portion of one of the slanted side walls~~.

Claim 5 (Original): The semiconductor element of claim 1, wherein the first MOS element includes:

a well of a first conductive type formed on the substrate;

a source region of a second conductive type formed in the well;

a drain region of the second conductive type formed in the well;

a gate electrode formed on the well of the first conductive type; and

a gate insulating layer interposed between the gate electrode and the well of the first conductive type.

Claim 6 (Original): The semiconductor element of claim 1, wherein a gate insulating layer of the first DMOS element includes a relatively thicker portion.

Claim 7 (Original): The semiconductor element of claim 5, further comprising:

a protection layer covering the first MOS element and the first DMOS element, wherein the protection layer has first and second contact holes that expose a source region of the first DMOS element and a drain region of the first DMOS element, and wherein the protection layer has third and fourth contact holes formed in the protection layer to expose the source region of the first MOS element and the drain region of the first MOS element;

a source electrode that contacts the source region of the first DMOS element through one of the first and second contract holes;

a drain electrode that contacts the drain region of the first DMOS element through the other one of the first and second contact holes;

a source electrode that contacts the source region of the first MOS element through one of the third and fourth contact holes; and

a drain electrode that contacts the drain region of the first MOS element through the other one of the third and fourth contact holes.

Claim 8 (Original): The semiconductor element of claim 1, further comprising:

a second DMOS element formed on the substrate opposing the first DMOS element; and

a second MOS element formed on the substrate opposing the first MOS element.

Claim 9 (Original): The semiconductor element of claim 8, wherein the second DMOS element includes a gate electrode having slanted side walls.

Claims 10-17 (Canceled).